

CLAIM AMENDMENTS:

Claim 1 (Canceled).

Claim 2 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said planarized region is a part of said surface of said silicon substrate which has been subjected to a planarizing process.

Claims 3 and 4 (Canceled).

Claim 5 (currently amended): A combined semiconductor apparatus, comprising:

a silicon substrate having an integrated circuit formed therein, the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit;

a planarized region defined over said rough or irregular surface of said silicon substrate, a flatness of the planarized region being not more than 10 nanometers;

a planarized film disposed over said planarized region; and

a semiconductor thin film disposed over said planarized film, the semiconductor thin film including a light-emitting element and being bonded on said planarized film, so that said semiconductor thin film is disposed above the

integrated circuit and said planarized film electrically connects said light-emitting element to said integrated circuit, wherein:

said semiconductor thin film is made of a compound semiconductor as a main material; and

a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process.

Claim 6 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said planarized film includes:

an electrically conductive layer contacting with said light-emitting element; and

an interdielectric layer formed in a region peripheral to said electrically conductive layer.

Claims 7 and 8 (Canceled).

Claim 9 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said semiconductor thin film has a common electrode layer on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor thin film, in which said light-emitting element is formed, and

said second surface of said semiconductor thin film is disposed on a side of said planarized region of said silicon substrate.

Claim 10 (Previously presented): The combined semiconductor apparatus according to claim 9, wherein said integrated circuit includes individual electrode terminals; and

said apparatus further comprising individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual electrode terminal.

Claims 11- 17 (Canceled).

Claim 18 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said light-emitting element is a plurality of said light-emitting elements arranged in said semiconductor thin film.

Claim 19 (Canceled).

Claim 20 (previously presented): An optical print head including the combined semiconductor apparatus of claim 5.

Claims 21-36 (Canceled).

Claim 37 (New) The combined semiconductor apparatus according to claim 6, wherein the interdielectric layer has the same thickness as that of the electrically conductive layer.

Claim 38 (New) The combined semiconductor apparatus according to claim 5, wherein an entire portion of the planarized film is directly disposed on an upper surface of said planarized region, and an entire lower surface of the planarized film contacts the upper surface of said planarized region.